AMENDMENT

Please amend the application as follows:

In the Claims:

Please cancel claims 3-6, 15-16, and 31-32 (claim 2 canceled previously). Please amend claims 1, 7, 14, 17, 30, and 33. The current version of all the claims follows:

1. (Currently amended) A receiver digital circuitry, comprising:

digital down-converter circuitry configured to mix a digital input signal provided by a receiver analog circuitry with a digital intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

digital filter circuitry configured to filter the digital down-converted signal to generate a filtered digital signal,

wherein the digital filter circuitry provides a notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry, and

wherein the digital filter circuitry provides the notch by using a notch filter circuitry that has one or more poles the locations of which are adjustable over an adjustment cycle of the notch filter circuitry, and wherein the locations of the one or more poles of the notch filter circuitry are adjusted in an initial part of the adjustment cycle of the notch filter circuitry so that the notch filter circuitry tends to settle quickly.

2-6. (Canceled.)

7. (Currently amended) The receiver digital circuitry of claim ~~6~~1, wherein the locations of the one or more poles of the notch filter circuitry are further adjusted in a latter part of the adjustment cycle of the notch filter circuitry so that the notch filter circuitry tends to produce a narrow notch.

8. (Previously presented) The receiver digital circuitry of claim 7, wherein the locations of the one or more poles of the notch filter circuitry are adjusted by modifying at least one filter coefficient of the notch filter circuitry.

9. (Previously presented) The receiver digital circuitry of claim 8, wherein the locations of the one or more poles of the notch filter circuitry are adjusted before a reception of a burst of data by the receiver digital circuitry begins.

10. (Previously presented) The receiver digital circuitry of claim 9, wherein the intermediate frequency local oscillator signal comprises a digital signal.

11. (Previously presented) The receiver digital circuitry of claim 10, wherein the digital filter circuitry further comprises:

a cascade integrator/comb filter circuitry configured to receive and filter the digital down-converted signal, the cascade integrator/comb filter circuitry further configured to provide a cascade integrator/comb filter circuitry output signal; and

a secondary filter circuitry configured to receive and filter the cascade integrator/comb filter circuitry output signal, the secondary filter circuitry further configured to provide the filtered digital signal.

12. (Previously presented) The receiver digital circuitry of claim 11, wherein the secondary filter circuitry further comprises the notch filter circuitry and at least one biquad filter circuitry configured to receive and filter an output signal of the notch filter circuitry.

13. (Previously presented) The receiver digital circuitry of claim 12 used in a radio-frequency transceiver circuitry.

14. (Currently amended) A radio-frequency (RF) receiver circuitry, comprising:

receiver analog circuitry included within a first integrated circuit, the receiver analog circuitry configured to receive and process a radio-frequency input signal to generate a processed radio-frequency signal, the receiver analog circuitry further configured to

use an analog-to-digital converter circuitry to convert the processed radio-frequency signal into a digital output signal; and

receiver digital circuitry, included within a second integrated circuit and coupled to the receiver analog circuitry within the first integrated circuit, the receiver digital circuitry configured to receive and process the digital output signal to generate a processed digital signal, the receiver digital circuitry further configured to provide a notch in a frequency spectrum of the processed digital signal,

wherein the receiver digital circuitry provides the notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry by using a notch filter circuitry configured to provide the notch, and wherein the notch filter circuitry provides the notch at minus a frequency of an intermediate frequency local oscillator signal.

15-16. (Canceled.)

17. (Currently amended) The radio-frequency receiver circuitry of claim ~~16~~14, wherein the notch filter circuitry has one or more poles the locations of which are adjustable so as to modify the settling time and notch width of the notch filter circuitry.

18. (Previously presented) The radio-frequency receiver circuitry of claim 17, wherein the locations of the one or more poles of the notch filter circuitry are adjusted at an initial point in time so that the notch filter circuitry tends to settle quickly.

19. (Previously presented) The radio-frequency receiver circuitry of claim 18, wherein the locations of the one or more poles of the notch filter circuitry are adjusted at least once more after the initial point in time so that the notch filter circuitry tends to produce a progressively narrow notch.

20. (Previously presented) The radio-frequency receiver circuitry of claim 19, wherein the locations of the one or more poles of the notch filter circuitry are adjustable by modifying at least one filter coefficient of the notch filter circuitry.

21. (Previously presented) The radio-frequency receiver circuitry of claim 20, wherein adjustment of the locations of the one or more poles of the notch filter circuitry completes before a reception of a burst of data by the receiver digital circuitry begins.

22. (Previously presented) The radio-frequency receiver circuitry of claim 21, wherein the intermediate frequency local oscillator signal comprises a digital signal.

23. (Previously presented) The radio-frequency receiver circuitry of claim 22, used within a radio-frequency transceiver circuitry.

24. (Previously presented) The radio-frequency receiver circuitry of claim 22, further comprising digital programmable gain amplifier circuitry configured to apply a programmable gain to the processed digital signal to produce a scaled digital signal.

25. (Previously presented) The radio-frequency receiver circuitry of claim 24, further comprising a baseband processor circuitry coupled to the receiver digital circuitry, the baseband processor circuitry configured to receive the scaled digital signal.

26. (Previously presented) The radio-frequency receiver circuitry of claim 25, used within a radio-frequency transceiver circuitry.

27. (Previously presented) The radio-frequency receiver circuitry of claim 24, further comprising digital-to-analog converter circuitry configured to convert the scaled digital signal to an analog signal.

28. (Previously presented) The radio-frequency receiver circuitry of claim 27, further comprising a baseband processor circuitry coupled to the receiver digital circuitry, the baseband processor circuitry configured to receive the analog signal.

29. (Previously presented) The radio-frequency receiver circuitry of claim 28, used within a radio-frequency transceiver circuitry.

30. (Currently amended) A method of receiving a radio-frequency (RF) signal, comprising:

receiving and processing the radio-frequency signal to generate an analog processed radio-frequency signal;

converting the analog processed radio-frequency signal to a digital signal; and

processing the digital signal by providing a notch at a frequency that corresponds to a residual DC offset in the analog processed radio-signal by using a notch filter circuitry that has one or more poles the locations of which are adjustable so as to modify the settling time and notch width of the notch filter circuitry, and wherein the notch filter circuitry has one or more poles the locations of which are adjustable so as to modify the settling time and notch width of the notch filter circuitry.

31-32. (Canceled.)

33. (Currently amended) The method of claim ~~32~~30, wherein providing the notch further includes adjusting the locations of the one or more poles of the notch filter circuitry at an initial point in time so that the notch filter circuitry tends to settle quickly.

34. (Previously presented) The method of claim 33, wherein providing the notch further comprises adjusting the locations of the one or more poles of the notch filter circuitry at least once more after the initial point in time so that the notch filter circuitry tends to produce a progressively narrow notch.

35. (Previously presented) The method of claim 34, wherein providing the notch further comprises adjusting the locations of the one or more poles of the notch filter circuitry by modifying at least one filter coefficient of the notch filter circuitry.

36. (Previously presented) The method of claim 35, wherein providing the notch further comprises completing the adjustment of the locations of the one or more poles of the notch filter circuitry before a reception of a burst of data by the receiver digital circuitry begins.

37. (Previously presented) The method of claim 36, further comprising applying a programmable gain to the processed signal to produce an scaled digital signal.

38. (Previously presented) The method of claim 37, further comprising providing the scaled digital signal to a baseband processor circuitry.

39. (Previously presented) The method of claim 37, further comprising converting the scaled digital signal to an analog signal.

40. (Previously presented) The method of claim 39, further comprising providing the analog signal to a baseband processor circuitry.